OptiMOS®-T Power-Transistor

AEC Qualified

RoHS

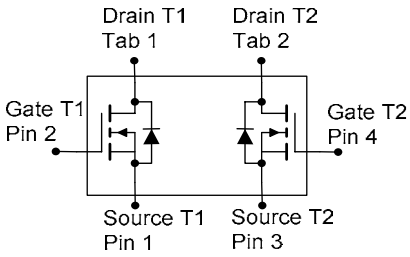
Product Summary

V_{DS}	55	V
$R_{DS(on),max}$ [5]	2 x 45	mΩ
I_D	15	A

Features

- Dual N-channel Logic Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

P-TDSON-8-4



Type	Package	Marking
IPG15N06S3L-45	PG-TDSON-8-4	3N03L45

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current one channel active	I_D	T_C=25 °C, V_{GS}=10 V [1]	15	A
		T_C=100 °C, V_{GS}=10 V [2]	12	
Pulsed drain current [2] one channel active	$I_{D,pulse}$	T_C=25 °C	60	
Avalanche energy, single pulse [2, 5]	E_{AS}	I_D=7.5A	47	mJ
Avalanche current, single pulse [5]	I_{AS}	-	15	A
Gate source voltage [4]	V_{GS}	-	±16	V
Power dissipation one channel active	P_{tot}	T_C=25 °C	21	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	7	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	100	-	
		6 cm^2 cooling area[3]	-	40	-	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D= 1 mA	55	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=10 µA	1.2	1.7	2.2	
Zero gate voltage drain current[5]	I_{DSS}	V_{DS}=55 V, V_{GS}=0 V, T_j=25 °C	-	0.01	1	µA
		V_{DS}=55 V, V_{GS}=0 V, T_j=125 °C[2]	-	1	100	
Gate-source leakage current[5]	I_{GSS}	V_{GS}=16 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance[5]	$R_{DS(on)}$	V_{GS}=5 V, I_D=6A	-	70	80	mΩ
		V_{GS}=10 V, I_D=10A	-	39	45	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance[5]	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	1090	1420	pF
Output capacitance[5]	C_{oss}		-	140	180	
Reverse transfer capacitance[5]	C_{rss}		-	130	195	
Turn-on delay time	$t_{d(on)}$	V_{DD}=27.5 V, V_{GS}=10 V, I_D=15 A, R_G=25 Ω	-	7	-	ns
Rise time	t_r		-	16	-	
Turn-off delay time	$t_{d(off)}$		-	24	-	
Fall time	t_f		-	34	-	
Gate Charge Characteristics[2, 5]						
Gate to source charge	Q_{gs}	V_{DD}=11 V, I_D=15 A, V_{GS}=0 to 10 V	-	6	8	nC
Gate to drain charge	Q_{gd}		-	3	4.5	
Gate charge total	Q_g		-	15	20	
Gate plateau voltage	$V_{plateau}$		-	5	-	V
Reverse Diode						
Diode continous forward current[2] one channel active	I_S	T_C=25 °C	-	-	15	A
Diode pulse current[2] One channel active	$I_{S,pulse}$		-	-	60	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=15 A, T_j=25 °C	-	1.0	1.3	V
Reverse recovery time[2]	t_{rr}	V_R=27.5 V, I_F=I_S, di_F/dt=100 A/µs	-	7	-	ns
Reverse recovery charge[2, 5]	Q_{rr}		-	9	-	nC

[1] Current is limited by bondwire; with an R_{thJC} =7 K/W the chip is able to carry 17A at 25°C.

[2] Specified by design. Not subject to production test.

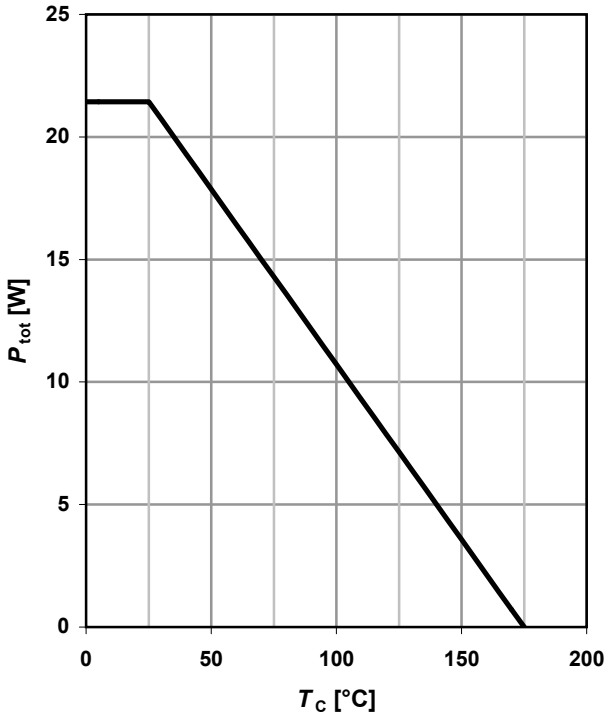
[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[4] Qualified at -5V and +16V.

[5] Per channel

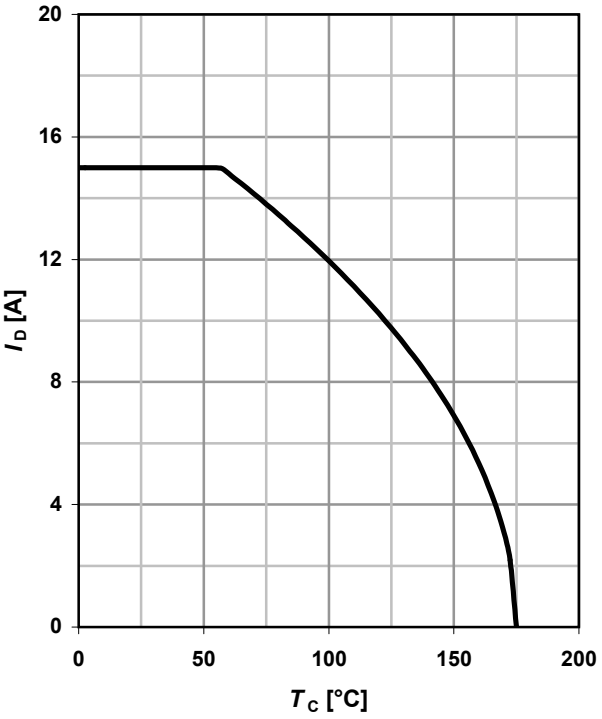
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V; one channel active



2 Drain current

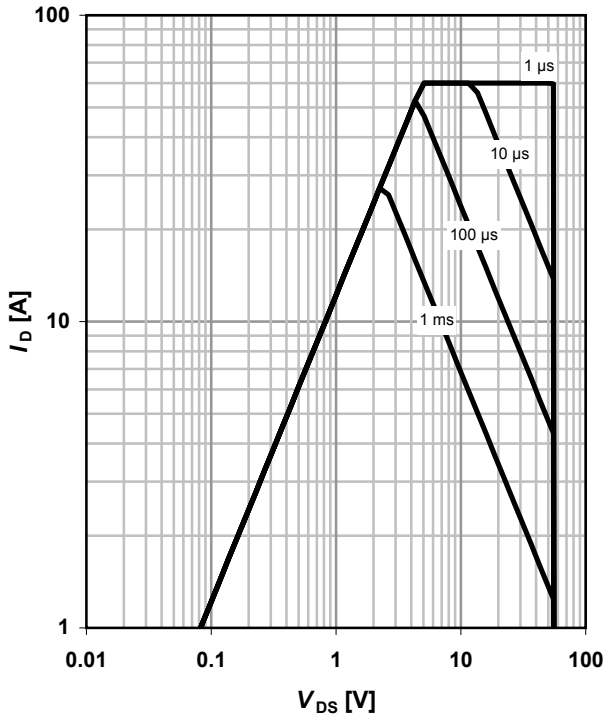
$I_D = f(T_C)$; $V_{GS} \geq 6$ V; one channel active



3 Safe operating area

I_D=f(V_{DS}); T_C=25°C; D=0; one channel active

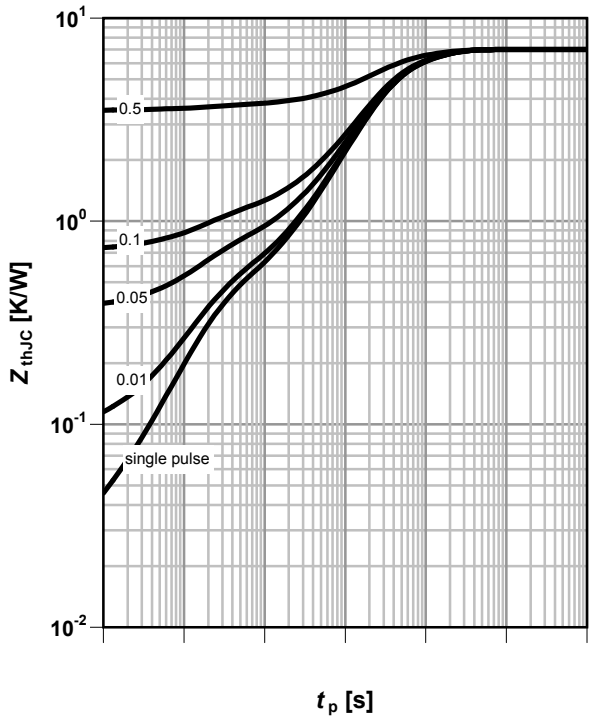
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

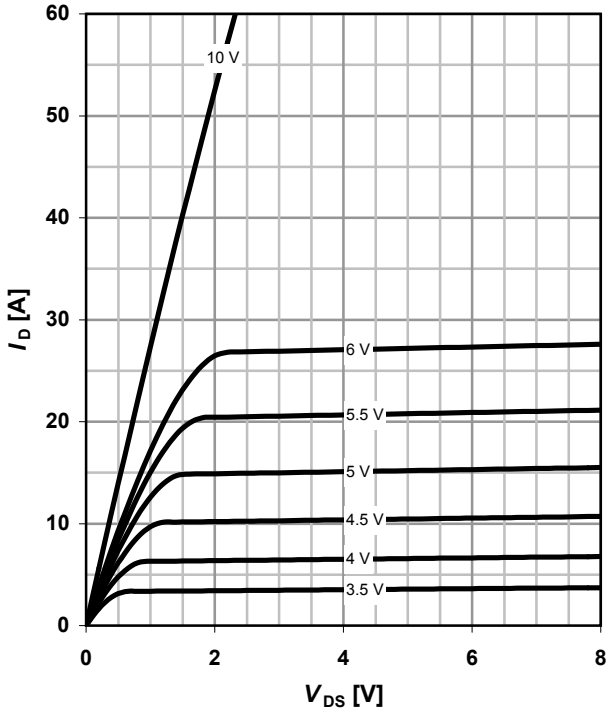
parameter: $D = t_p/T$



5 Typ. output characteristics[5)]

$I_D = f(V_{DS})$; $T_j = 25$ °C

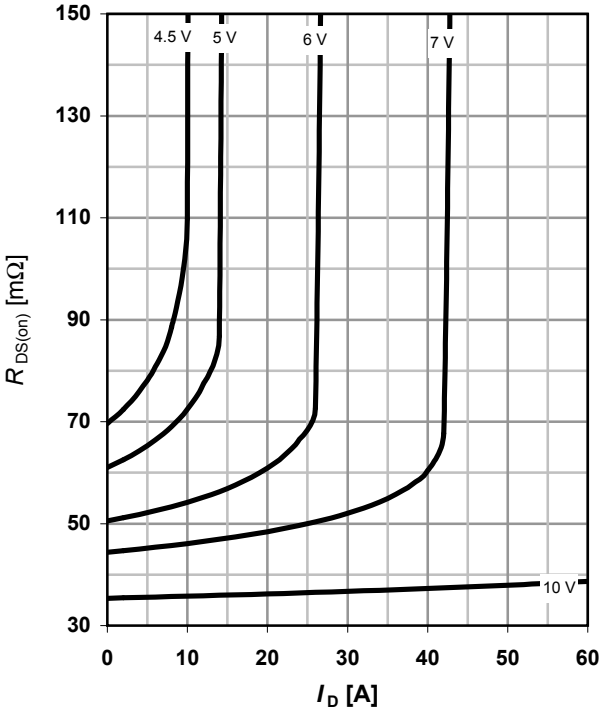
parameter: V_{GS}



6 Typ. drain-source on-state resistance[5)]

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C

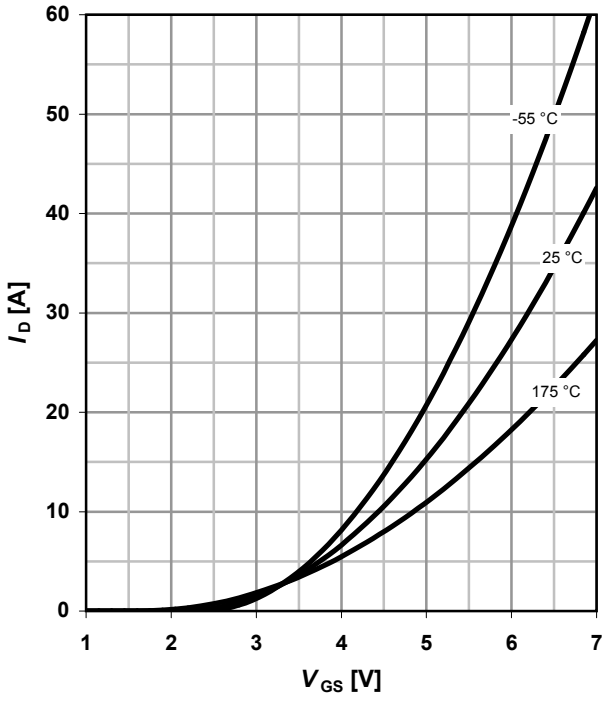
parameter: V_{GS}



7 Typ. transfer characteristics[5)]

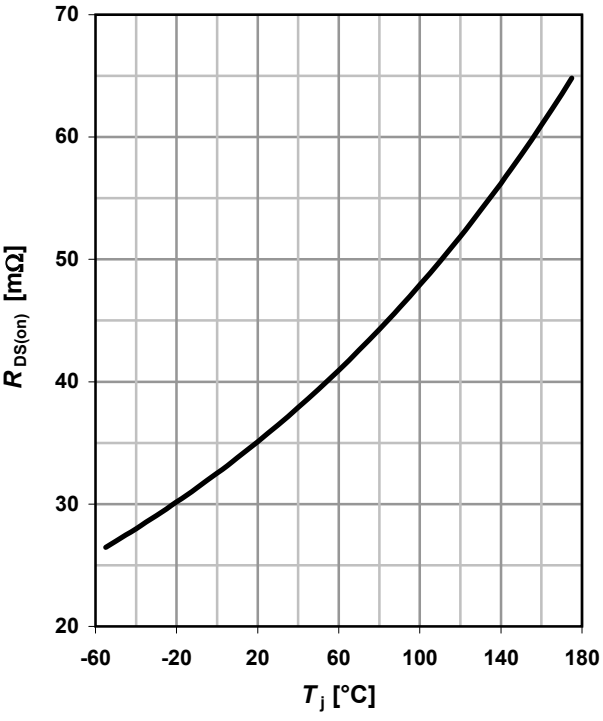
$I_D = f(V_{GS})$; $V_{DS} = 6$V

parameter: T_j



8 Typ. drain-source on-state resistance[5)]

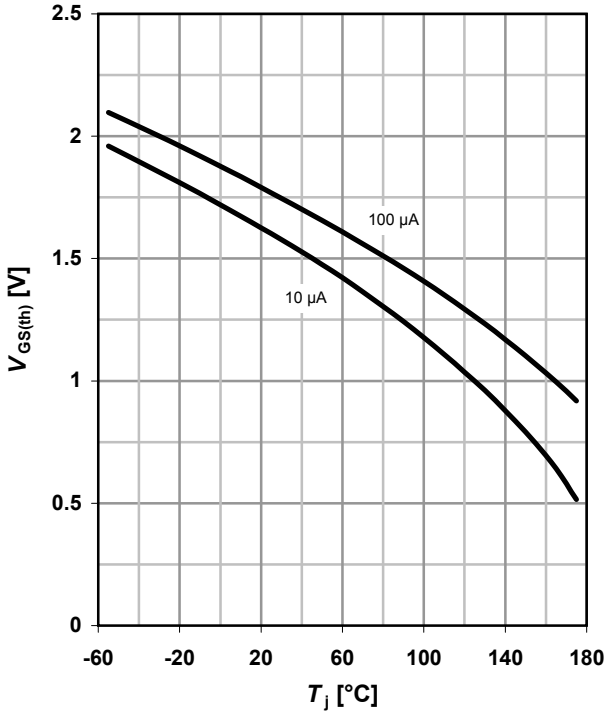
$R_{DS(on)} = f(T_j)$; $I_D = 10$ A; $V_{GS} = 10$ V



9 Typ. gate threshold voltage

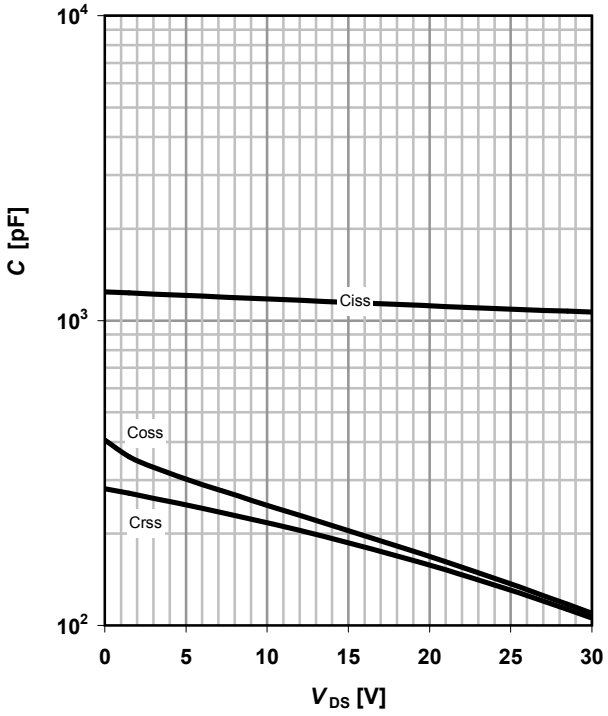
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. Capacitances[5)]

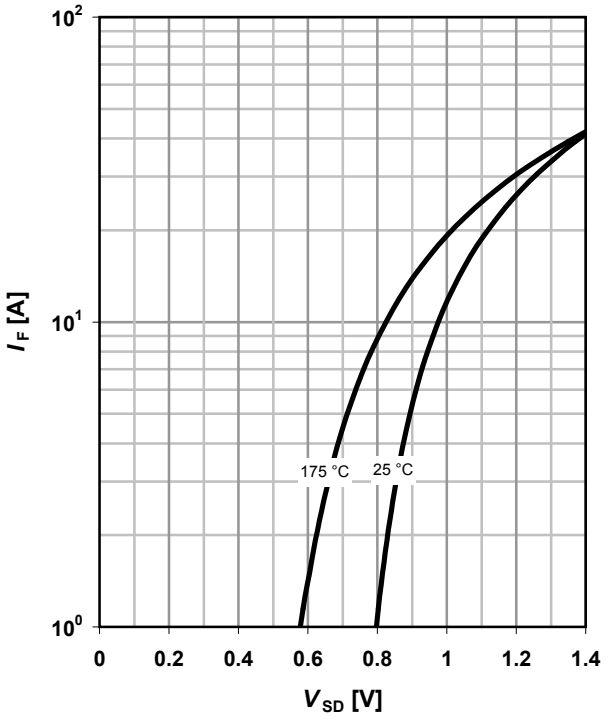
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis[5)]

IF = f(V_{SD})

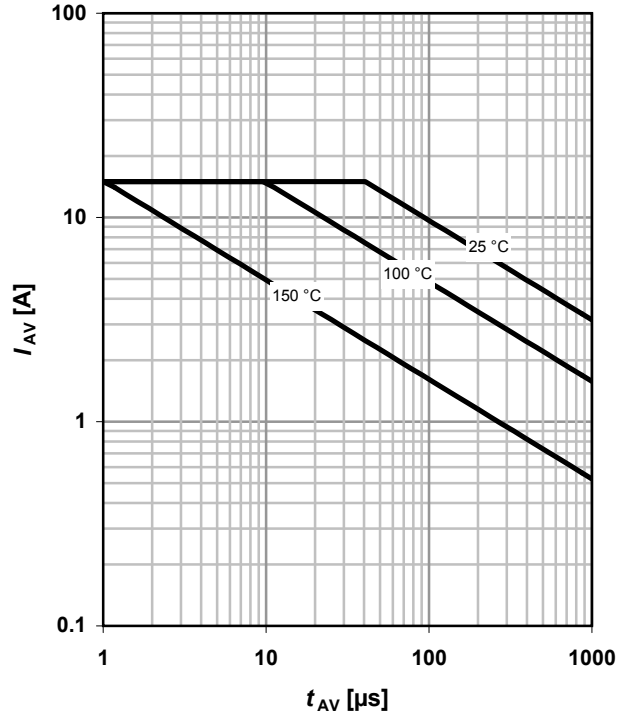
parameter: T_j



12 Avalanche characteristics[5)]

$I_{AS} = f(t_{AV})$

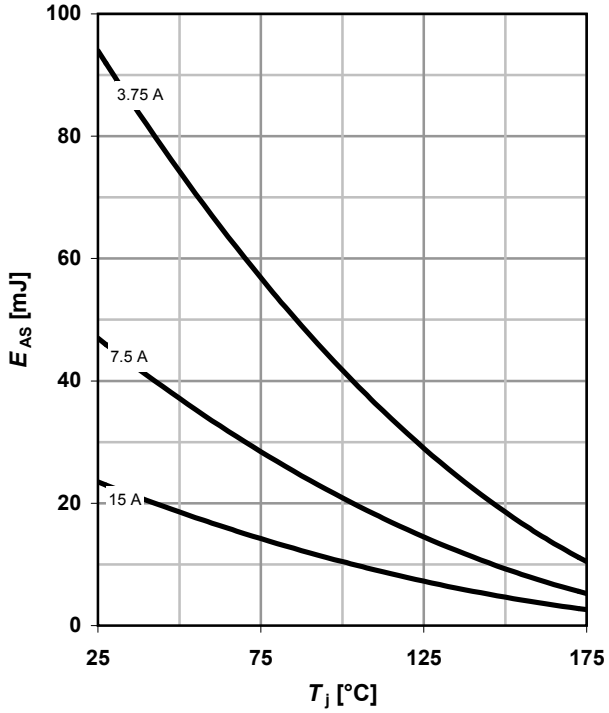
parameter: $T_{j(start)}$



13 Avalanche energy[5)]

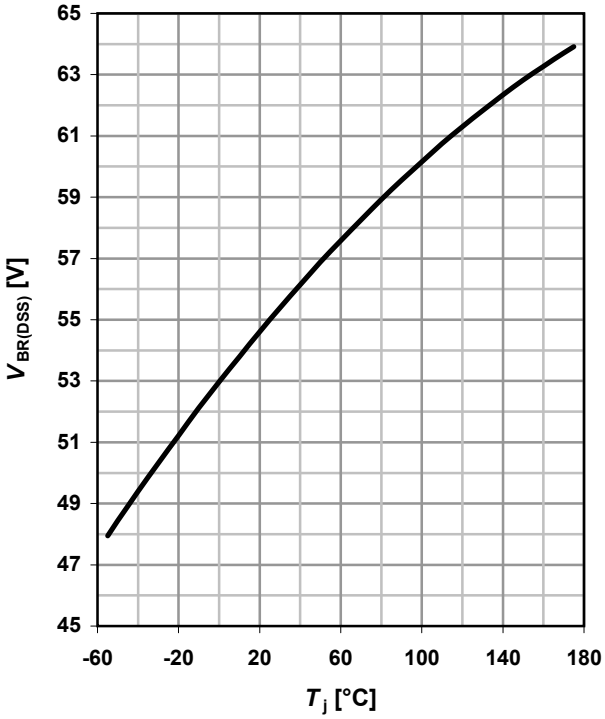
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

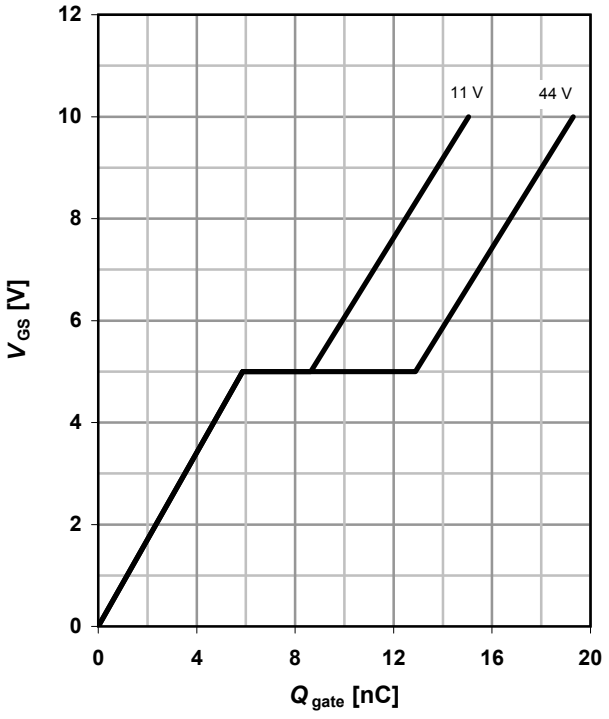
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



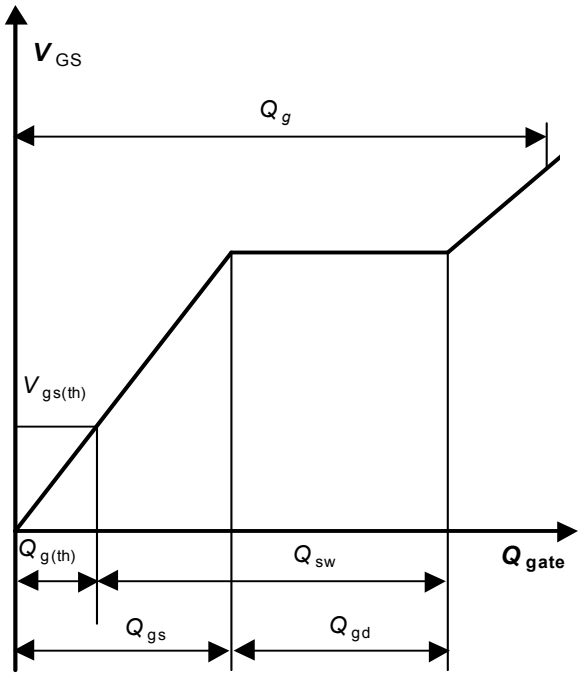
15 Typ. gate charge[5)]

$V_{GS} = f(Q_{gate})$; $I_D = 15$ A pulsed

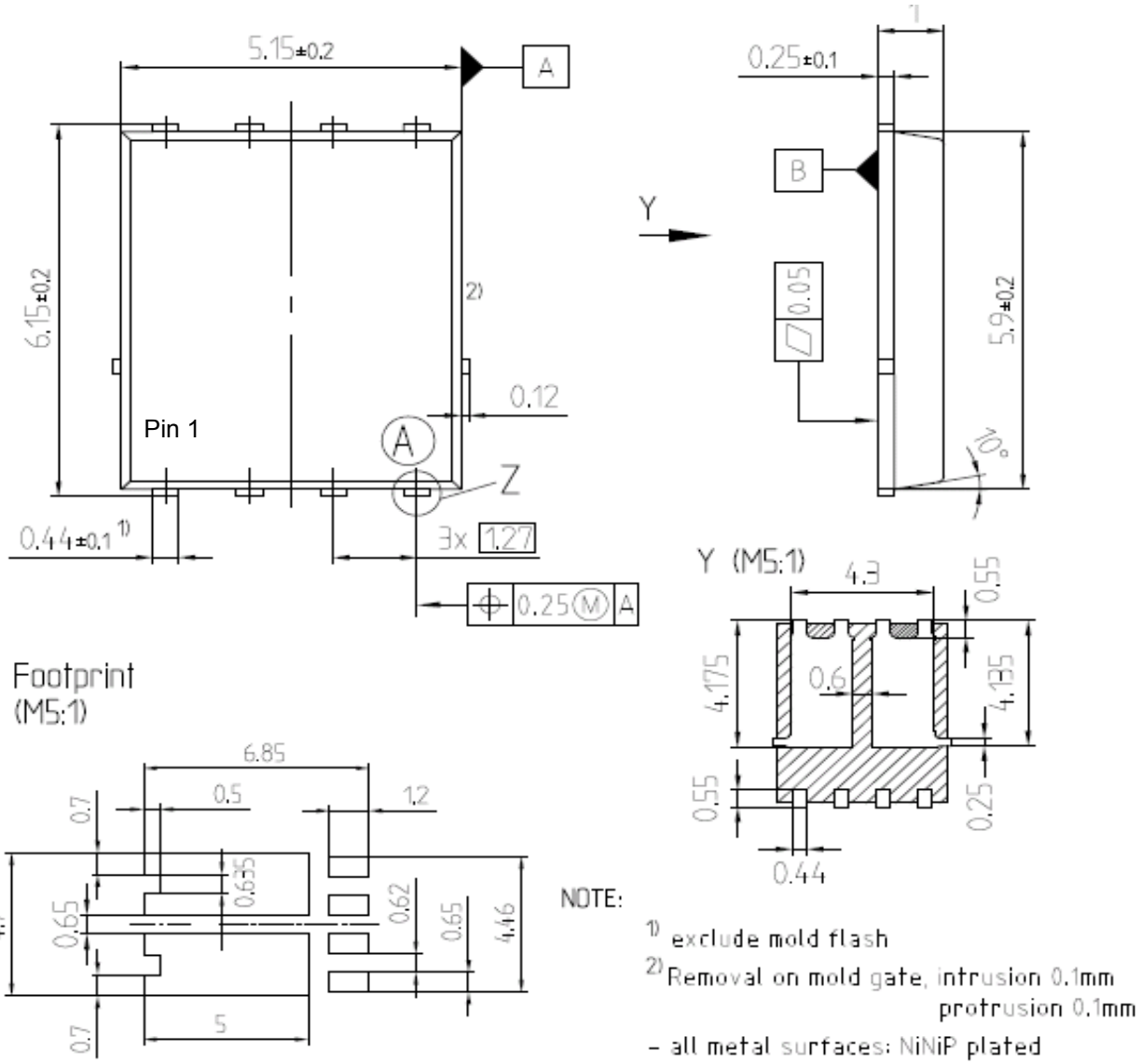
parameter: V_{DD}



16 Gate charge waveforms



Package Outline



Dimensions in mm

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Revision History

Version	Date	Changes
Revision 0.1	08.12.2007	Initial Target Data Sheet
Revision 0.2	07.04.2008	Update of disclaimer, package drawing, layout according latest disclaimer
Revision 0.2	07.04.2008	Update of capacitances
Revision 0.2	07.04.2008	Condition Id Ron 5V and 10V updated
Revision 0.2	07.04.2008	Condition Id for Eas updated
Revision 0.3	08.05.2008	Initial Preliminary Data Sheet